

Flying Probe Tester

# DESIGN *for* Testability



**Handbook**

# Contents

## ■ Flying Probe tester – Design for testability

Overview	3
What is testability?	4
<i>Which are the advantages of testability?</i>	4
<i>No contact, no testing</i>	4

## ■ Rules for the mechanical design

Overview	5
Mechanical requirements	6
<i>Board dimensions</i>	6
<i>Height of components</i>	6
<i>Board conveyance</i>	7
Fiducial	7
<i>Position</i>	7
<i>Shape and dimensions</i>	8
Contact points typology	9
<i>Test Pad</i>	9
<i>Via</i>	9
<i>Via inscribed in a pad</i>	10
<i>Via followed by one pad</i>	10
<i>Soldering pad of SMT components</i>	10
<i>Pins of traditional components (PTH)</i>	11
<i>Table</i>	11
Quantity of contact points	12
Power supplies contact points	12
Use of fixed probes	13
<i>Test Pad</i>	13
<i>Test pads dimension</i>	13
<i>Test pads arrangement</i>	13
<i>Distance between the test pads</i>	13
<i>Reference holes</i>	14
<i>Vias</i>	14
Panel of boards	15
<i>Fiducial</i>	15
<i>Panels typology</i>	15
<i>Use of the bed of nails</i>	15
Ceramic substrates	16

## ■ Rules for the board accessibility

Overview	17
Board accessibility	18
<i>Contact side</i>	18
<i>Choosing the contact side</i>	18
<i>Contacting from the top side</i>	18
<i>Contacting from the bottom side</i>	19
<i>When contacting the board from the top side?</i>	20
<i>When contacting the board from the bottom side?</i>	20

## ■ Rules for the electric design

Overview	21
Initialization circuit	22
Oscillators	22
Digital integrated circuits	22
Analog integrated circuits	23
On Board Programming	23
<i>In system write</i>	23
<i>Direct programming</i>	23
<i>Disabling the Microprocessor</i>	23
<i>Signals accessibility</i>	24
ECO	24
Boundary Scan	25
<i>Boundary Scan Infrastructure</i>	25
<i>Boundary-scan chain</i>	25
<i>Fully IEEE-1149.1 Compatil devices</i>	25
<i>TAP signal noise</i>	25
<i>Boundary-scan chain connection</i>	25
<i>Let Boundary-scan chain breakable</i>	25
Board level design	26
<i>TCK clock quality</i>	26
<i>Power Supply filtering</i>	26
<i>BSDL file availability</i>	26
<i>Met compilance enable condition</i>	26
<i>Pin numbering in board netlist</i>	26
CAD Files	27
<i>Supported CAD formats</i>	27

## ■ Design for Testability Milestones

Overview	28
Design for Testability Table	29-30



# Flying Probe Tester Design for Testability

How is it possible to ensure the good functioning of a product without testing it?

At least the functions to satisfy the Client's expectations need to be tested.

"Flying Probe Tester - Design for Testability" assists the designers of electronic boards, in order to make boards easy to be tested besides being manufactured.

The access to the test pads, their dimensions and their number are more and more important characteristics, because of the restrictions imposed by the miniaturization reached by electronic components.

This document is about mechanical and electrical accessibility, and the simplification of its electrical testing.

This guide, as a reference, allows reducing time and expenses, to prevent situations that can be solved in advance.



### What is testability?

Testability can be defined as the convenience to check a board or a component, with the expected level of precision.

How can it be easy verifying the correspondence between the specifications and the real functioning?  
How fast can it be the generation of a test program?  
How accessible can the components be?

Which level of diagnostic covering can be ensured?  
Answering these questions allows defining the testability of an electronic board.

Testability is a technological rationalization.

This way to conceive the products creates the consciousness of how important it is to think about easy testing. ... during the product engineering ... the production ... the practice of the products themselves.

As long as it is introduced during the design phase, the testability enables reducing test expenses and time.

### Which are the advantages of testability?

The most evident advantages of following the "design for testability" criteria to design boards are in terms of time and money.

Further advantages are (but not only): best efficiency and test accuracy, and more profitability.

Design for testability enables:

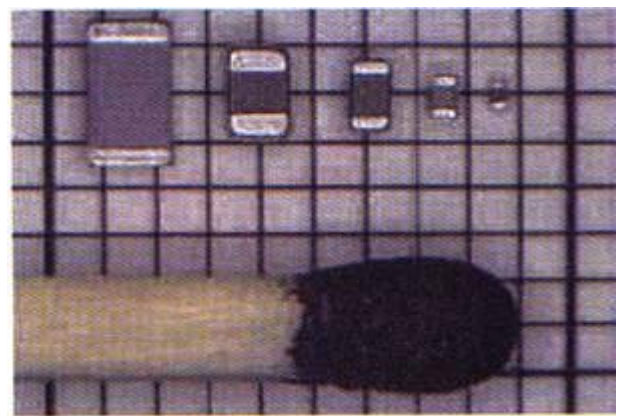
- To reduce the time needed to pass from the design to the production.
- To reduce the designers getting involved during the production start-up.
- To improve the knowledge exchange and the cooperation among design technicians, engineers and production.
- To reduce the starting and normal expenses of the production cycle.
- To guarantee a best pins or components diagnostics, and, consequently, the reduction of the repair mean time.

### No contact, no testing

The technology of superficial mounting modified the type of boards in the world electronic production.

The components produced with SMT technology are smaller and smaller: they are mounted on both sides of the printed support and their density increases continuously, attaining objects that were inconceivable few years ago.

To understand the levels of miniaturization allowed by technology, it is enough to compare the passive components with package 1206 (still in use) and the most advanced 0201.



The physical bump contacts space needed by the traditional bed of nails contact technology, has been reduced and, in some particular applications with special technologies, it disappeared (as, for example, the mobile phones).

How is it possible to contact the components in order to check them?

By using the flying probes, which allow touching the inner points of the board. The flying probes technology enables to test the boards without needing a special bed of nails adapter.

The four flying probes move independently in the X, Y and Z planes, so they can touch the smallest targets with the maximum accuracy and repeatability.

When high accuracy and reduced dimensions are required, the concepts of testability must be applied since the board design.

The background of the entire page is a detailed, high-resolution image of a printed circuit board (PCB). Overlaid on this is a semi-transparent, stylized image of a flying probe tester. The tester consists of two main vertical arms, each with a probe at the end, positioned to test a component on the board. The text is overlaid on this background.

# Flying Probe Tester: Directions for the mechanical design

The performance of the flying probes test systems overcomes the mechanical characteristics of the bed of nails systems and it gives the possibility to test electronic boards equipped with the new miniaturization technologies and components implementation.

During the board design phase, it is important to know that some choices can be very important and that they can have important consequences on the testability and accessibility of the board.

As the electronic designers learned some rules to make the boards manufacturing easier (as, for example to make different the mounting sides of components in SMT and traditional technology) it is important that they acquire some rules of mechanical design, to make the board testing easier.

*It is important to pay attention to the fact that the minimum dimensions defined in this document are referred to the 4040 model “Top-of-class”, the state-of-art flying probe.*

*For the other flying probe models (“High Precision” and “Very High Precision”) the minimum dimensions change with the system characteristics.*

# Mechanical requirements

## Board dimensions

To be tested on a SPEA 4040 flying probes system, the board must be included in one of the following dimensions:

- 20x16" (500x400mm)
- 24x24" (610x610mm)
- 27x24" (686x610mm)

In accord to the system test area.

## Height of components

The components mounted on the tested side must be lower than 60 mm, otherwise the probes will not be able to fly over them.

On the side opposite to the tested one, there must not be components higher than 60 mm, otherwise the board cannot be conveyed.

Anyway, with flying probes testers with shuttle, it is possible to convey boards with components 110 mm high.

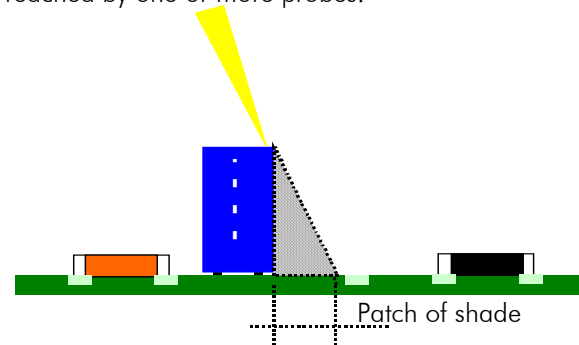
The positioning of components much higher than others (for example, electrolytic capacitors, transformers, ...) is a matter that needs particular care already during the board design phase.



If the side chosen to perform the contact is the side where components are mounted, the components could block the probes movement.

It is suggested to collect all the components of this type in a provided area of the board or, at least, to share them out in groups.

Their height can block the probes movement, and it creates some patches of shade that cannot be reached by one or more probes.



In this case it is necessary not to place contact points in these areas and taking in consideration the following table:

Component height	Minimum dimension free from contact points
5 mm	1.4 mm
10 mm	2.8 mm
15 mm	4.2 mm
20 mm	5.6 mm
25 mm	7.0 mm
30 mm	8.4 mm
35 mm	9.8 mm

For systems with shuttle (boards manual loading), it is necessary that they have areas free from components minimum 15x7mm for each one of the fixing points.

In this way, it is possible to use the shuttle standard blocking mechanisms.





## Rules for the mechanical design

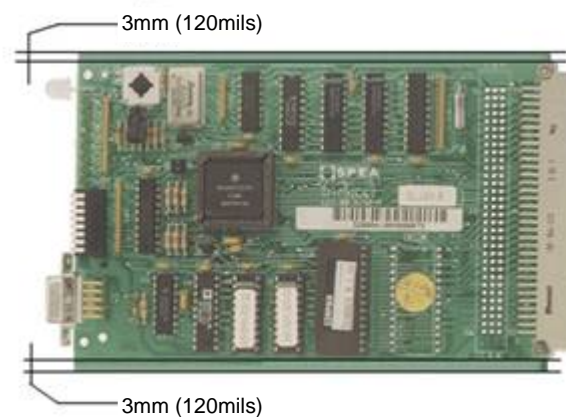
If the board has an irregular profile, use the additional magnetic blocking mechanisms.



### Board conveyance

To convey the boards through automatic in line board loader (IBL) it is necessary to follow the directions reported below:

The room on the sides used for the conveyance must not be less than 3 mm, so the board blocking and stopping mechanism can operate without problems.



For the board conveyance on automatic line, two solutions are available:

- Standard, to convey boards with weight up to 1500 gr
- Specific, to convey boards with weight up to 2500 gr

## Fiducial

Fiducial is one smooth shape, it is repeatable and positioned at the same coordinates on all boards.

The 4040 flying probe test system has an optical board position detector similar to what is available on equipments of automatic insertion of “pick and place” components, and, usually, both equipments use the same fiducials.

The 4040 optical alignment system allows checking the real positioning of the board on the conveyance system, it adjusts also any positioning inexactness and non orthogonally.

The fiducial has to be described in the CAD files, in the part list, in the net list and in the list of the coordinates.

### Position

It is suggested to position at least two fiducials on the opposite corners of the board diagonal.



The fiducials must be positioned asymmetrically, so, the optical detection system can correct both the board rotation and any offset. If the board is rotated of 180°, the recognition will fail.

Position the fiducials on both sides of the board, even if the components are mounted only on one side.

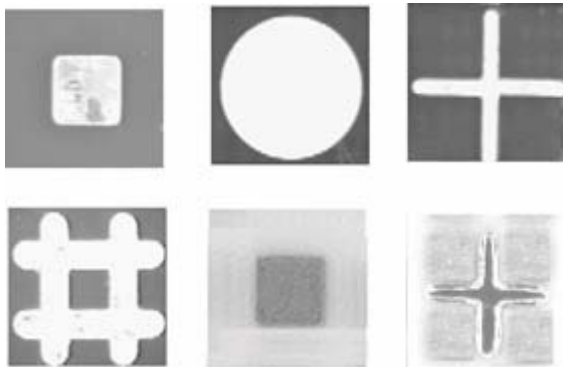
Considering that in these cases the test is performed from the side with no components, there have to be fiducials in this side too.

## Rules for the mechanical design

### Shape and dimensions

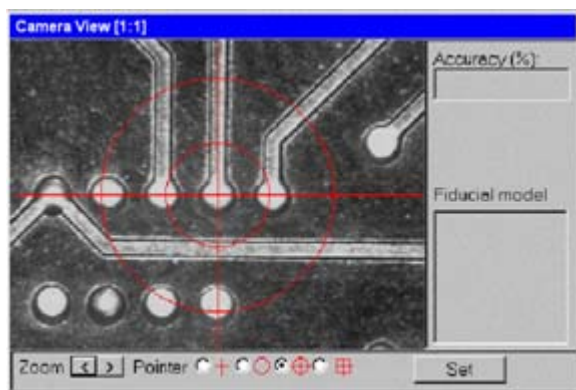
The 4040 flying probe tester fiducials optical recognition can share and recognize every shape of fiducial. To obtain the best results, it is better to use fiducials of the following types:

- Round
- Square
- Cross-shaped



To be recognized as a fiducial, it must be univocal inside the area (11x9 mm) framed by the video camera during the search.

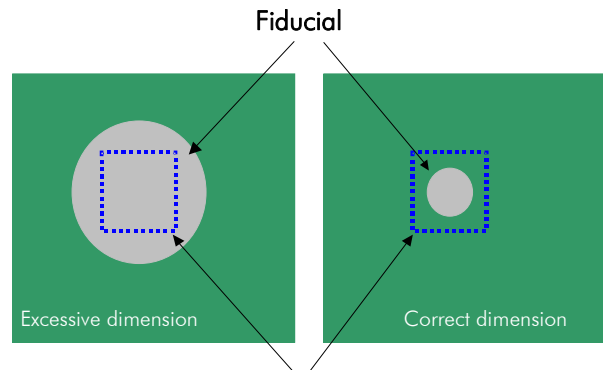
Otherwise, the fiducial searching program could be unable to identify the correct fiducial.



The previous image is an example of points that cannot be used as fiducial because they are very similar.

The maximum dimensions of the area that includes the fiducial are 4.5x4.5 mm.

In case the size of the area is bigger than as described above, the recognition could fail or it can be ineffective.

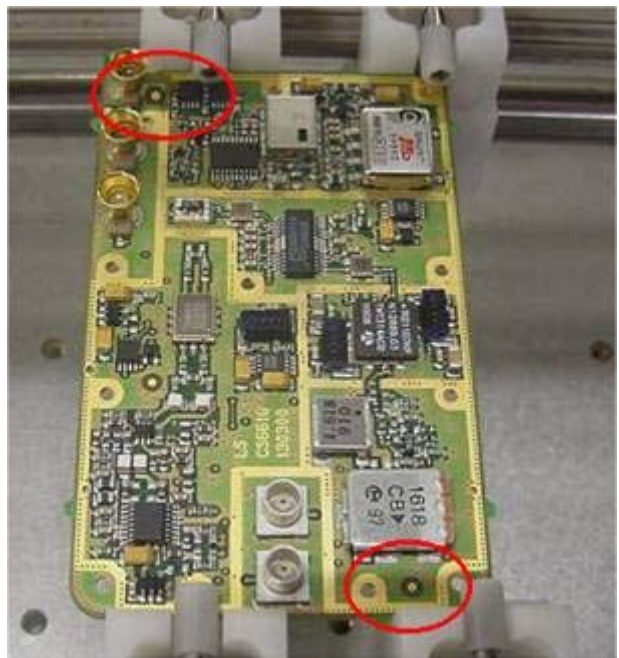


Area of the fiducial

A good recognition of the fiducials is one of the parameters to attain the expected flying probes positioning accuracy. This is why it is suggested to arrange an area without components, vias, tracks not smaller than 1 mm<sup>2</sup> around the fiducial in order not to affect the image of the fiducials.

This is the reason why the fiducial must not be covered by tin and it must be far from parts that can reflect the light (e.g.: screens, connectors with metallic body, ...).

The light reflected would affect the image used for its recognition.





### Contact points typology

The boards tested on flying probes system require some easy (and not expensive) rules of mechanical design, which can improve testability and make it easy.

#### Test Pad

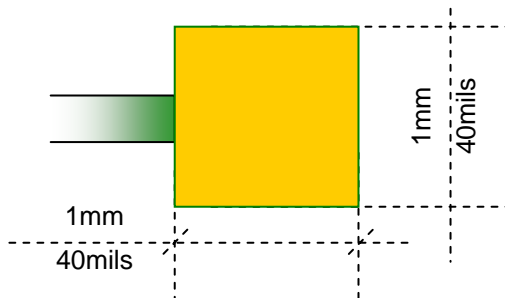
The test pad is metallic, ideally golden, preferably squared (or round) and exclusively devoted to the test.

To guarantee the contact, the test pads must be covered by conductive material and they must not be subject to oxidation.

So, the contacting quality is ensured also if the storage times between the mounting and the testing of the board are long.

If these characteristics are satisfied, the test can be a perfect contact point example.

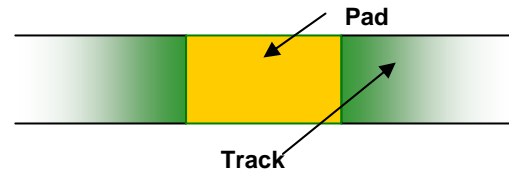
The test pad suggested dimensions are of one millimeter each side, even if it is possible to perform the contact with test pads of 20mils (500 $\mu$ m) and, occasionally, with test pads smaller than 10mils (250 $\mu$ m).



If necessary, the flying probes can contact in repeatable way test pads up to 3mils (80 $\mu$ m). This presupposes some conditions as: board planarity, probes calibration, fiducials typology and all the other related issues

In brief, the ideal contact is obtained with square golden pads of 1mm per side.

If we take into consideration the 4040 high precision, accuracy and repeatability, the test pads can be obtained by uncovering, from the solder resist, small parts of track in the external layer chosen to perform the contact.



In this case, the track width must not be less than 4mils (100 $\mu$ m). It should be possible to use tracks with dimensions up to 3mils (80 $\mu$ m) but, practically, the board and printed circuit manufacturing processes cannot assure this kind of accuracy.

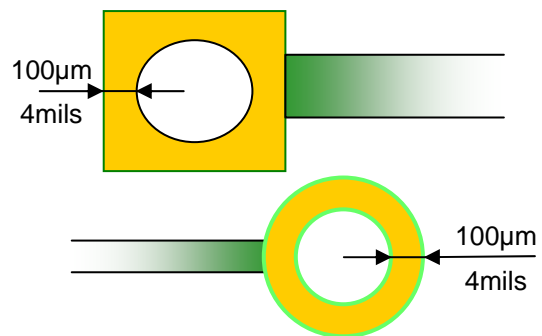
#### Via

The effective and repeatable contact of the vias, needs the metallic edge to be without solder resist; if golden, the via would be preferred. Observing only these rules, does not make vias good contact points.

When the probes contact the vias, they have the attitude to "strike" inside the hole, with the risk of being caught or of damaging the point.

For this reason, it is suggested to solder the via: it would become, covered with tin, a test pad and the contact would be easier.

If it is not possible to cover the vias with tin (for example for the chosen production process), it is suggested to make them square, not round. This would mean more space to perform the contact.



SPEA developed probes devoted to contact the vias.

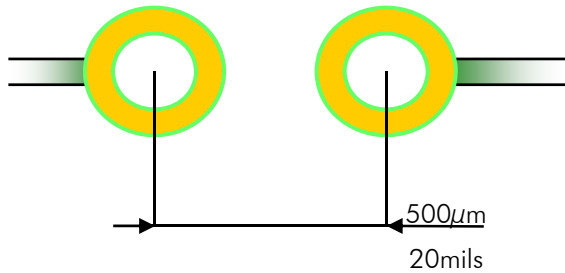
Their head is pyramid-shaped, so they can touch the edge of the hole.

In this case it is possible to ensure a minimum pitch of 20mils (500 $\mu$ m) or 33mils (800 $\mu$ m) in accord to the used via hole and used spring probe.

## Rules for the mechanical design

If the via is going to be used as a contact point, the minimum size of the metallic area must not be less than 4mils (100  $\mu\text{m}$ ), in order to guarantee the contact repeatability.

The minimum pitch, to be guaranteed between two vias, depends on the type of probe used; anyway, it must not be less than 20 mils (500  $\mu\text{m}$ ); even if 4040 can obtain better results, up to 10mils (250 $\mu\text{m}$ ).

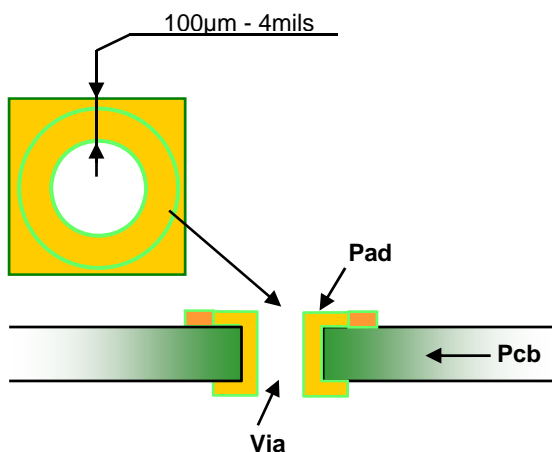


In brief, the use of the via as a contact point can be a choice (in this case, the holes will be tinned and fit probes will be used to perform the test) or a makeshift solution.

There are some expedients which can enable to transform a via in a acceptable and reliable contacting point.

### Via inscribed in a pad

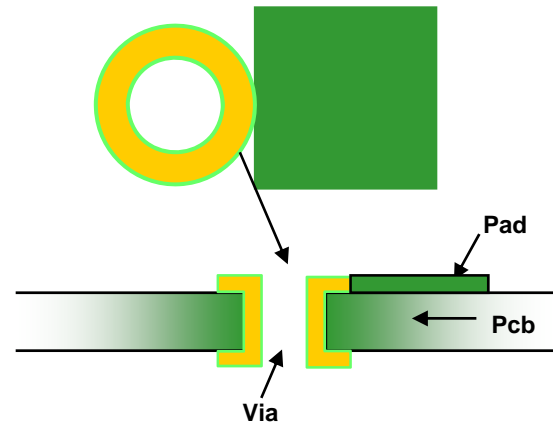
It is possible to have more contact surface available (easier contact) by inscribing the via in a square pad.



To guarantee the contact repeatability, the minimum metallic area suggested must not be less than 100  $\mu\text{m}$ .

### Via followed by one pad

By increasing one side of the via metallic crown, it is created one test pad positioned near the via hole.



The pad's suggested dimensions are those suggested for the test pad.

### Soldering pad of SMT components

One rule to make the contact of the components' soldering pads easier, is to provide for pads "prolonged" as regards to the soldering needs, during the PCB disentangling.

The required space is the space needed to contact the probes; it must be plane, to ensure a stable and safe contact during the test.



Soldering pads typical geometry



Soldering pads suggested geometry

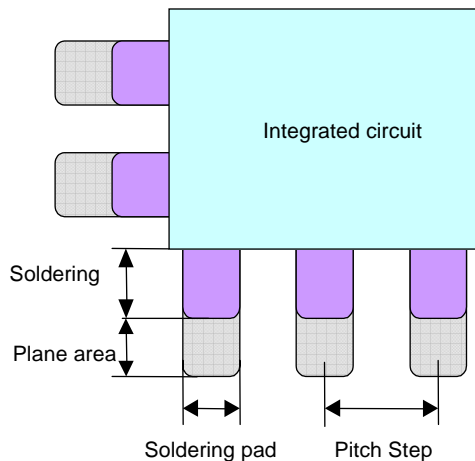
After being introduced in the CAD-CAE libraries, the modification of the dimensions of the soldering pads does not mean much more work for the designers, but it means having very positive boards testing results.

Contacting on soldering pads has to be taken into consideration with attention; its priority is subordinate to the test pads.

About integrated circuits in SMD technology, it must be considered that with the contact on pins, it could seem that also that the cold soldering is valid.

The shrewdness suggested to contact soldering pads through the 4040 flying probes system need to observe the following dimensions:

- Pad width:  $\geq 100 \mu\text{m}$
- Pad length:  $\geq 100 \mu\text{m}$
- Pitch :  $\geq 250 \mu\text{m}$



The values previously listed concern the suggested dimensions, for adequate contact.

The performances of the 4040, according with some factors that can positively influence the contact, can allow reducing the suggested dimensions:

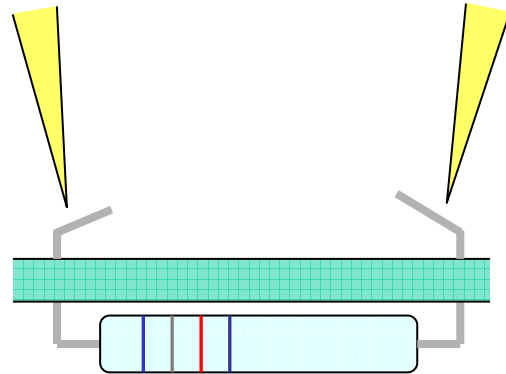
- Type of spring contact
- Fiducial precision and typology
- Board planarity
- Boards conveyor planarity

It should be possible to use soldering pads of reduced dimensions up to 3mils ( $80\mu\text{m}$ ) but, practically, the board and printed circuit manufacturing processes have to assure this kind of accuracy.

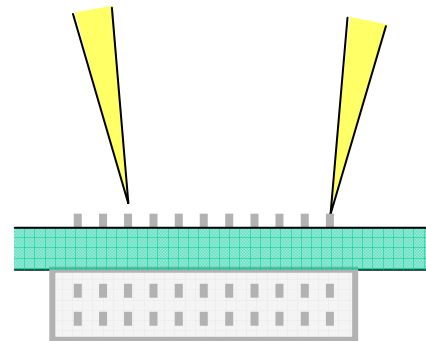
### Pins of traditional components (PTH)

The pins of the components in traditional technology (PTH), are not always a good contact point, this depends in particular on the presence of the rheophore of the component.

If the pins are not “levelled” to a predefined length, the rheophore could interfere with the probe movement and cause inexactness of the probe positioning and its wearing.



Vice versa, the pins of “levelled” components (as, for example integrated circuits, connectors, ...) ensure enough contact reliability.



### Table

The main rules concerning the contact points characteristics are listed in the following table:

	Test Pad	Via	SMT Pad
Suggested dimension	1x1 mm	1x1 mm	1x1 mm
Minimum dimension	$\Phi 250 \mu\text{m}$	$80 \mu\text{m}^{(1)}$	$80 \times 80 \mu\text{m}$
Suggested shape	Square	Square	Rectangular
Acceptable shape	Round	Round	Rectangular
Suggested pitch	$500 \mu\text{m}$	$500 \mu\text{m}$	$500 \mu\text{m}$
Minimum pitch	$250 \mu\text{m}$	$250 \mu\text{m}$	$250 \mu\text{m}$

<sup>(1)</sup> = Metallic crown width



### Quantity of contact points

To ensure the expected diagnostic covering of a test program, each net of the board must be contactable at least in one point.

Examples of contact points that can be used by the 4040 are:

- Test pads
- SMT components soldering pads
- Pins of traditional components (PTH)
- Vias

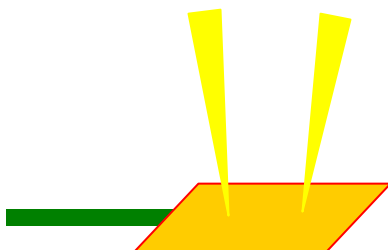
To test in the best way, it is suggested to provide at least one more contact point for the nets connected to:

- Capacitors with value higher than  $10\ \mu\text{F}$
- Diodes of low-medium power ( $I_f > 50\ \text{mA}$ )
- Resistors with value less than  $100\ \Omega$
- Bipolar transistors
- Mos-Fet transistors
- Relays
- Fuses
- Transformers
- Inductances

In general, it is suggested to provide two contact points for all the components working with currents of more than 1 A, and to provide one more contact point for each next current unit.

If it is not physically possible to provide more than one test pad per net, the only contact point must be not smaller than the maximum suggested size (1x1 mm) or, better, it could be bigger.

In this way, two probes can have simultaneous access to the same contact point (to remedy to the lack of the second point).



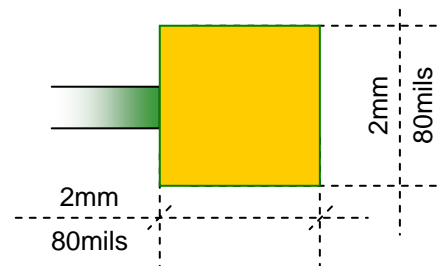
### Power supplies contact points

The nets to supply the boards need particular considerations for what concerns their accessibility.

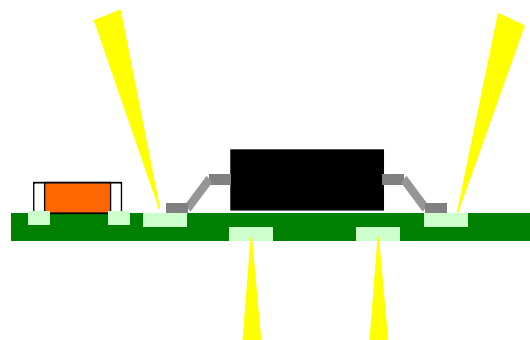
For example, two available contact points are needed to ensure the best measurements.

Since contact on the supply nets is performed many times during the test (even hundreds of times), it is better to provide at least ten contact points uniformly arranged above the board surface. In this way, it is possible to program the flying probes in order to allow them joining the contact point with the shortest movement possible.

Furthermore, at least some test pads should be, if possible, squared; their dimensions should be 2x2 mm and they should be positioned as near as possible to the board edges.



In this case, it is suggested to provide the access from both sides of the board, to allow contacting without considering the side used to test.



The suggested directions enable to contact both with single spring contacts manually positioned, and with bed of nails.

### Use of fixed probes

It is possible to provide, already during the design phase, for the employment of fixed probes with flying probes.

Their connection to the test system channels can be performed both through connectors and through special pneumatic or vacuum bed of nails.

It is suggested to follow some directions since the board design, in order to employ the possibility to use the fixed points in the best way.



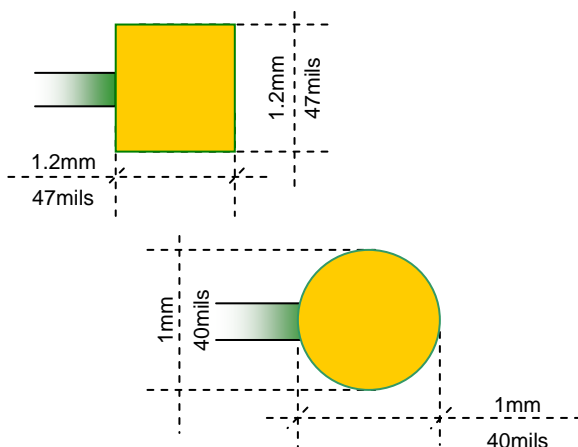
If the contact is performed in the side opposite to the one contacted by the flying probes, some directions about dimensions and pads arrangement would help to realize the bed of nails.

### Test Pad

The test pad is completely devoted to the test, so it guarantees the spring contacts used by the bed of nails.

### Test pads dimensions

To ensure proper and repeatable contact, the test pads should be square and their side should be 1.2mm; it is anyway acceptable having a round test pad with 1mm diameter.

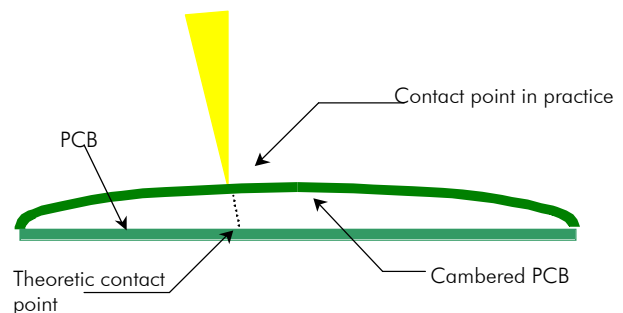


Even if it is possible to contact test pads with 0.8mm diameter, it is suggested not to use them.

In this case, it would be necessary to use spring contacts with 1.27 mm (50 mils) step, which last nearly 10 times less than "standard" types, being twice as expensive.

### Test pads arrangement

The test pads have to be uniformly arranged on the board surface: if located in few areas of the board, the board could be cambered in anomalous way.



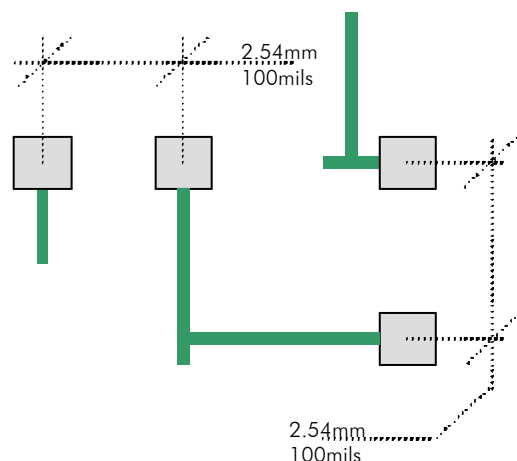
The 4040 flying probes are not perfectly at right angles to the board plane (the external probes are 16° and the internal 5° angular).

As shown in the previous figure, if the board is deformed, it is not possible to guarantee the 4040 contact precision.

### Distance between the test pads

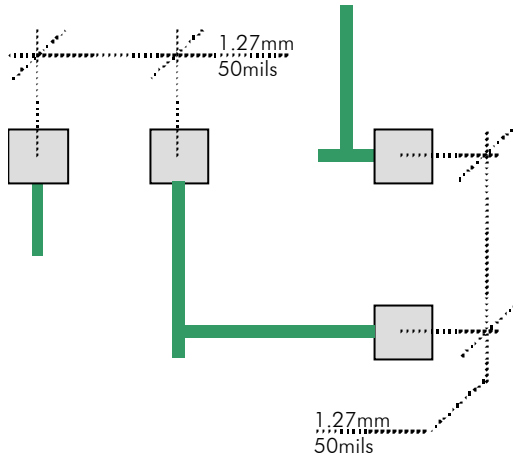
To be contacted with repeatability and efficiency, the suggested distance between the test points is, 2.54 mm (100 mils).

In this way, it is possible to use "standard" spring contacts with 2 mm diameter, which ensure repeatable contact.



## Rules for the mechanical design

If for any reason (e.g.: the layout) it is not possible to guarantee the distance of 2.54 mm between the test pads, do not place them at a distance less than 1.27mm (50mils).

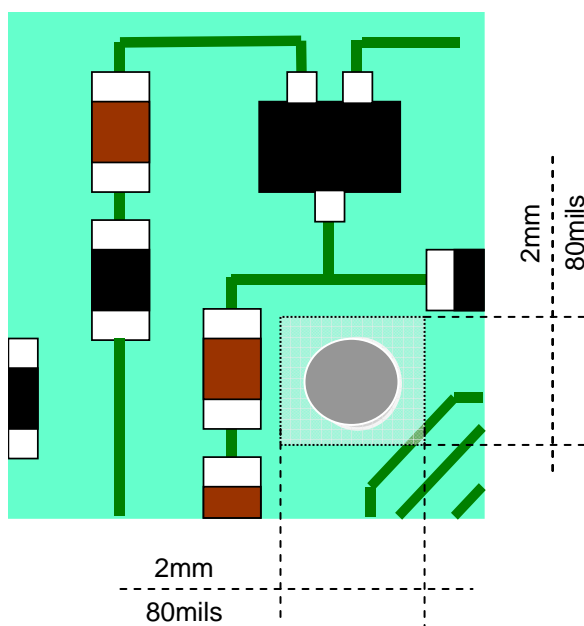


With this distance between the test pads it is no more possible to use standard spring contacts, but it is necessary to use specific contacts with reduced diameter (this type of spring contacts lasts less than the standard ones).

### Reference holes

The reference holes on the board help the operator that performs the test to position it on the bed of nails (reduced handling time).

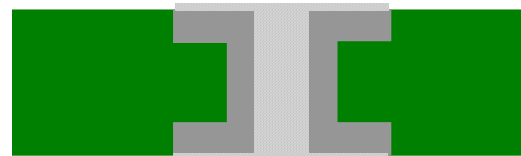
It is suggested to leave an area with side of 2 mm without components around the reference holes.



### Vias

As written in the preceding chapters, the vias are not a good contact point. They can be accepted if used with fixed probes (spring contacts), following some directions during the production process.

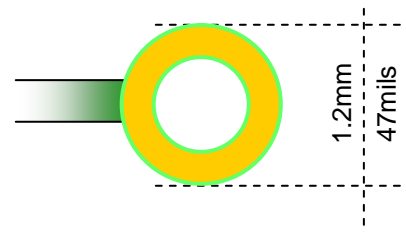
It is suggested, for example, to cover the via with tin during the soldering stage, in this way it could be assimilate to a test pad.



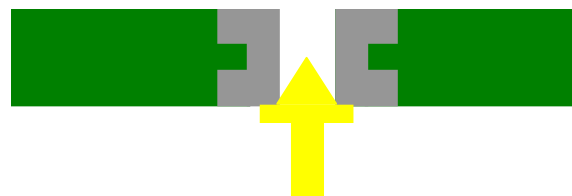
The average of density of the components on the boards to be tested, sometimes does not allow to cover with tin the vias during the soldering stage.

In these occasions, the considerations of the preceding chapters concerning the vias inscribed or followed by a pad are in force.

Anyway, the minimum size of a via to be used as a test point is the same of the test pads: their diameter must not be less than 1.2 mm.



Using standard spring contacts with pyramid head, the repeatability is allowed (the probe is perfectly perpendicular to this one).



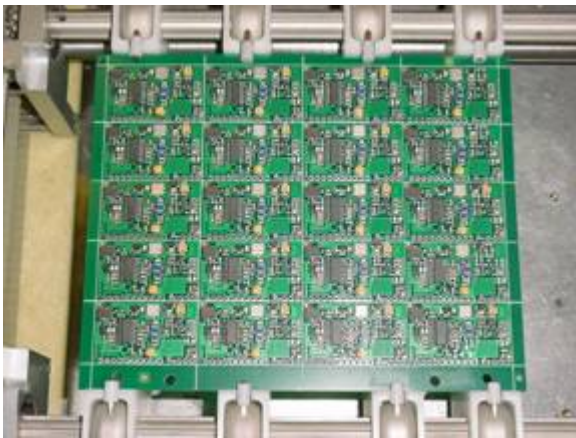


### Panel of boards

The 4040 flying probes test system can automatically contact panels of boards.

The panels of boards can consist in different boards configurations, for example identical boards with identical rotation, or with different rotation, different boards, ...

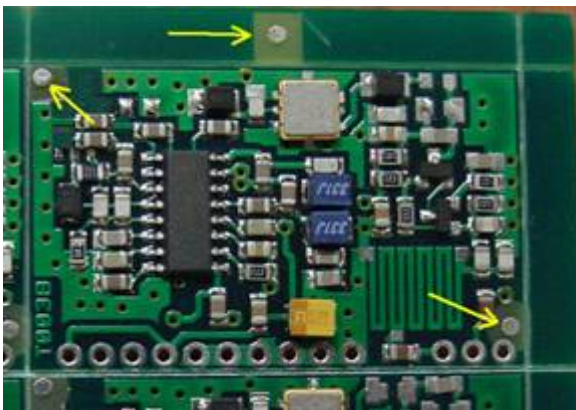
Especially in case of panels of boards, it is important to follow the suggestions available in this document; any problem detected on one board influences all the boards that are part of it.



### Fiducial

It is suggested to position at least one couple of fiducials on the whole panel and one couple for each board that constitutes it.

This enables the expected accuracy and repeatability values of the probes positioning.



### Panels typology

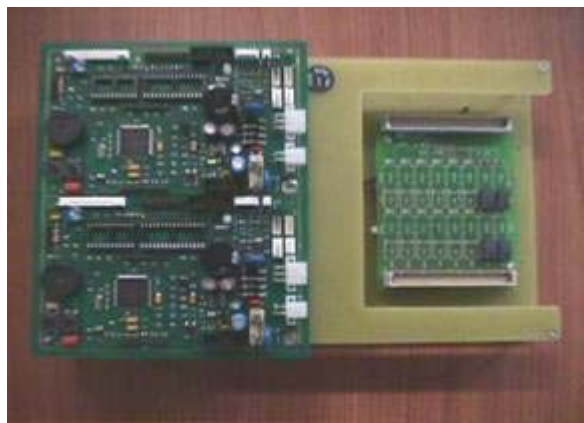
During the design of one panel of boards, it is suggested to follow the indications reported below:

- The panel must be composed by maximum 128 boards
- Reduce as much as possible the width of the "scoring" space between the boards
- The boards rotation must be identical
- The boards must be identical
- The offset must be identical between all the boards



### Use of the bed of nails

The bed of nails allows having access through spring contacts to the board inner points. The force that they will wield will be multiplied by the number of the boards of the panel.

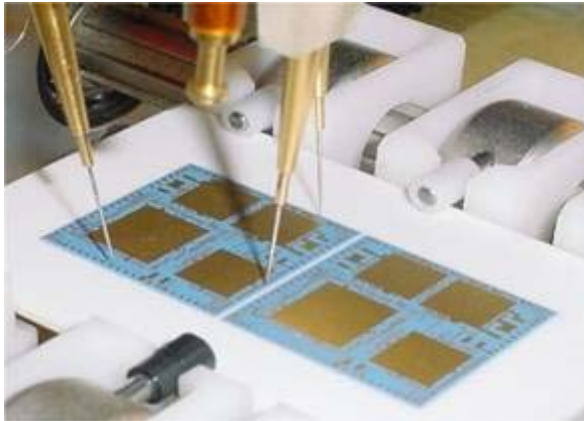


Considering this aspect, it is possible to prevent the board deformation caused by the force of the spring contacts.

## Rules for the mechanical design

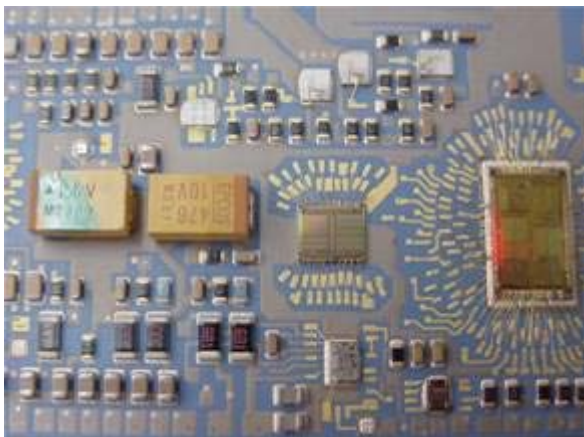
### Ceramic substrates

The 4040 flying probe tester has been designed in order to guarantee the contact with flying probes of ceramic substrates without damaging the pad devoted to testing or bonding.



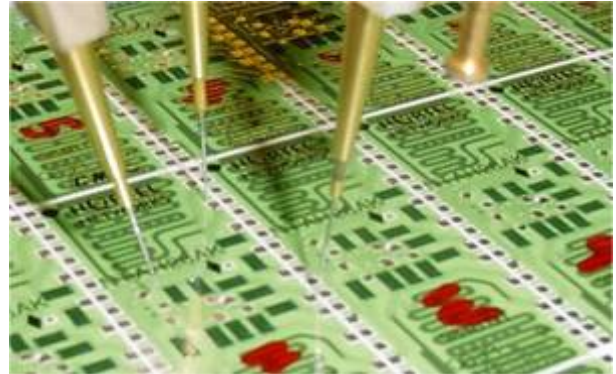
The speed of the probes on the Z axis is programmable: it can be programmed in order to reduce the speed in the last part of the down-stroke. This function is called “soft landing” and it allows exerting only the force of the probe spring.

This movement slackens the test crossing time; in order to employ the tester characteristics of speed and productivity, it is suggested to provide for contact pads.

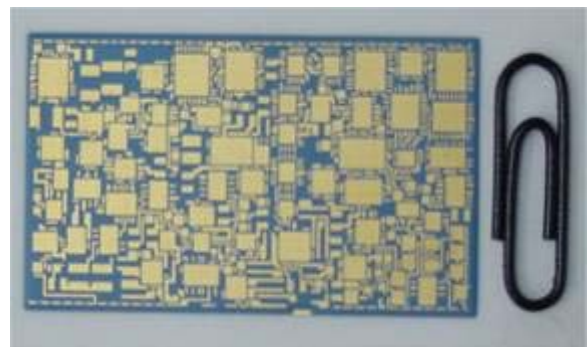


This would finally avoid deformations and scratches of the pad devoted to the bonding and it means a reduction of the mechanical resistance to the tug and the increasing of the electrical resistance in the laying point of the thin wire.

The test pads have very good contact properties because they are realized with the same serigraphy material of the “conductor” (palladium-silver or platinum-gold).



All the previous considerations about shape, quantity, step, typology have to be considered also for the testing of ceramic substrates.





# **Directions for the board accessibility**

The best advantage of the flying probes testers is the possibility of testing one board without needing the specific adapter.

It has to be taken into consideration that the miniaturization of the boards sometimes excludes the possibility to realize the bed of nails adapter.

During the design of one board it is necessary to remember that "no contact means no testing".

Contacting the board nets is fundamental to satisfy the expected level of quality and test covering.

How choosing the contact side?

What is involved in the choice of one side instead of another?

This chapter contains the answers to these questions.



### Board accessibility

All the considerations contained in this document can be applied to “medium” boards. This is to refer to boards having ordinary problems and not to particularities or exceptions. It is suggested to perform a technical analysis of each case.



The incomplete access to the nets of the board is the cause of the board production costs increasing: it would be better if each net of the board had more than one contact point. So, the test system will be able to measure and verify the board completely.

#### Contact side

One of the main rules of the Design for testability is to provide for the arrangement of all the test points on only one side of the board.

This is the reason why it is suggested to provide for the test pads positioning on the side (top or bottom) of the board where there are few components.

Usually the bottom side (soldering) is suggested for the contact.

The possibility to fly over the side with less components allows the probes moving closer to the board, and testing will be faster. If all the test points are located on the same side, the test program will not need subsequently board handling.

For this reason, if the board cannot be contacted only on one side, it is suggested that the number of test points of the secondary side is 10% if compared to the other.

#### Choosing the contact side

The choice of the side to be contacted is very important for the test strategy; undervaluing this choice means complexity in the test program development and disappointing diagnostic covering.

The choice should be well-pondered already during the design phase, not to have consequences on the test program.

Choosing the contact side influences the test strategy and the wished test depth.

For example, if it has been decided to test one board by contacting the bottom side (soldering), it will not be possible to perform simultaneously the optical test on components mounted above the opposite side (top-components).

Only fixed ElectroScan probes (instead of those provided on the flying probes) can test the proper soldering of the pins of the integrated circuits mounted on the components side.

Whereas, if we suppose to test one board from the top side (components), it is possible to find traditional components: they could hamper or not allow the access to some contact points.

#### Contacting from the top side

Even if the board was not designed following the “Design for Testability” criteria, contacting from the Top side (components), allows a best access to the nets.

The boards are very often produced with “mixed” technology, which includes components of “SMT” and “PTH” (traditional) technology.

The test program must take into consideration the possibility to have access problems because of traditional components that could hamper or not allow reaching some areas.

The presence of PTH components influences also the probes movement, which is different on a board with no “obstacles”; it can also influence the test program time execution.



Since the majority of the components is mounted on this side of the board, it is possible to perform the optical test.

The Electro Scan vectorless technique can be applied using the detectors located on probes 2 and 3, in this way there is no need of fixed probes.

The ElectroScan technique on the top side is suggested when there are integrated circuits with dispelling metallic plate. Its “shield” effect is avoided by the possibility of moving the detector probe near the lead frame of the component.

It is important to highlight that, if the board has few access points on the bottom side (soldering), for some nets, it is possible to realize a simple contacting tool.

This allows increasing the test points used simultaneously to test the board. The four flying probes are integrated by the “fixed” points of the bed of nails.

Few probes movements mean reduced test time while the use of fixed points (bed of nails or connectors) increases the program diagnostic covering.

An important aspect of board contact, which unfortunately is not always considered, is the cleaning of the board after the soldering stage.

It happens very often that if the boards are not washed after the soldering, a layer of material that cannot be scratched by the point of spring contacts remains above the board.

The point of the probes used for the contact has a reduced diameter which does not always allow the perfect perforation of the layer of flux.

Furthermore, these residual products could “dirty” the points of the probes and this could cause measuring inaccuracy.

This is most evident on the top side: the number of components makes the cleaning more difficult.

The presence of “ultra fine pitch” or “fine pitch” components highlights this condition.

### Contacting from the bottom side

The choice to contact one board from the bottom side (soldering) allows having easier access to the test points also with the flying probes; rarely, there can be PTH components hampering the probes movement.

Contacting the board from the bottom side enables programming the probes in order to make them fly over the board at few millimetres from it, reducing, in this way the test time.

Having few parts mounted on this side is not a negligible fact.

The positioning of the contact points is easier during the design and disentangling of the printed support.

## Rules for the board accessibility

The presence of the most part of components on the opposite side makes the optical test less effective or it could require to repeat the test.

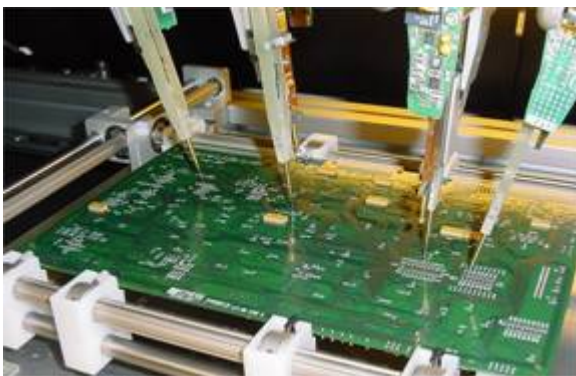
The ElectroScan vectorless technique is possible by using some fixed probes instead than the detectors located on the flying probes axes.



Contacting the board from the bottom side, it becomes more difficult to realize the bed of nails, because of the opposite side, where the majority of components are located.

This is the reason why it is important to respect the suggested dimensions of the test pads (square, 1.2 mm side).

Even if the contact is performed from the easier side, the cleaning must be considered anyway.



The flux residual products, or the used soldering paste can increase the probes contact resistance: the expected measurement accuracy could not be ensured for low resistances.

## When contacting the board from the top side?

To summarize, it is suggested to contact from the top side if the conditions listed below are observed:

- All the nets, or the majority of them can be contacted from this side
- There is no residual material of the previous working phases on the boards
- The dimensions of the contact points observe the Design for testability criteria
- There are no particularly bulky components to be avoided during the probes movement
- The test strategy needs the optical test and the detection of the unsuccessful soldering of pins of the integrated circuits
- Wish to use a specific bed of nails adapter.



## When contacting the board from the bottom side?

Summarizing, it is suggested to contact the board from the bottom side if the following conditions are observed:

- All the nets, or the majority of them can be contacted from this side
- The dimensions of the contact points (test pads, vias, soldering pads, ...) observe the Design for testability criteria
- The test strategy does not need the optical test
- It is not necessary to verify the soldering of the pins of the integrated circuits through detectors located on the flying probes
- It is not necessary to use a special bed of nails adapter





# **Directions for the electric design**

If taken into consideration and applied during the design of boards, electronic modules and printed circuits, the subjects contained in this chapter can help to define simple and uniform rules to simplify the test.

This concept has to be reminded: the test of the board influences every produced unit and all the units recognized as "faulty" during their working life.

It is important to understand and define rules, which, if followed since the first phases of design allow improving the quality and the reduction of the costs of the board during all production stages, including the test.

## Rules for the electric design

## Initialization circuits

The initialization (or reset) circuits allow defining the board status.

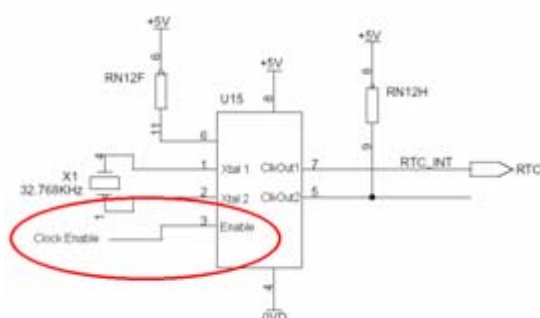
This usually happens during the board switching on and should be normally programmed during the usual functioning.

The first operation that any board with logic on board should be able to perform is the initialisation. It allows disabling the components that could alter the conditions on some points of the board.

It is suggested to design the board in order to make the reset condition easy to be activated; for example, forcing one point to a defined electrical level.

# Oscillators

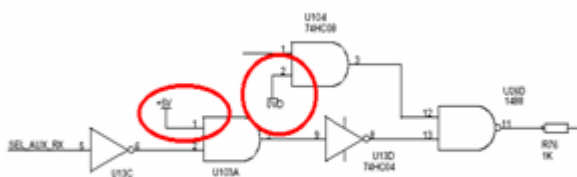
The test of circuits connected to oscillators can become easier if the oscillator is connected to a circuit through a jumper or an enabling pin.



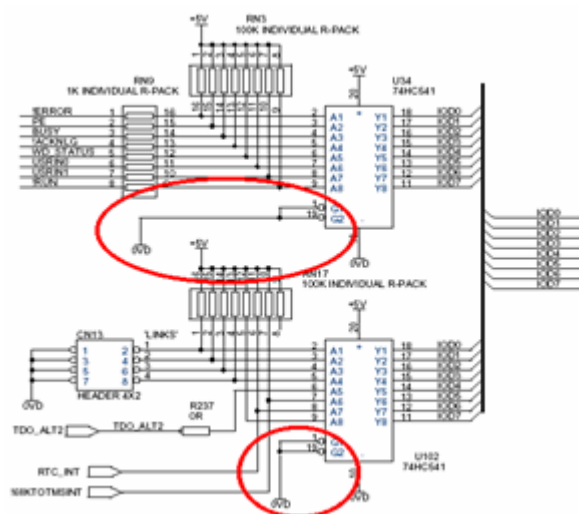
# Digital integrated circuits

During the In Circuit test, each component is tested individually through stimuli on its input and controlling pins.

This is the reason why it is not suggested to tie its pins directly to the power supplies or to the ground: the test system could not insulate or control them.



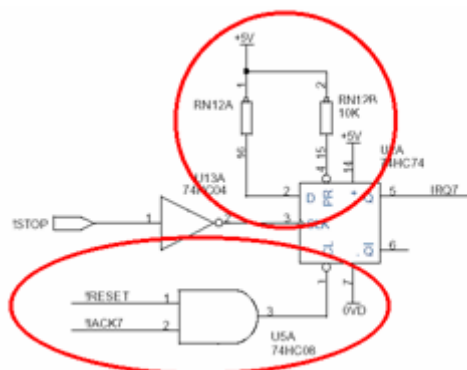
Another example of connection that does not allow testing the components properly is the following:



In this case, if digital “backdriving” is not correctly executed, the buffer, whose “Enable” pin is directly connected to the ground, could be cause of unsteadiness while testing the rest of the circuit.

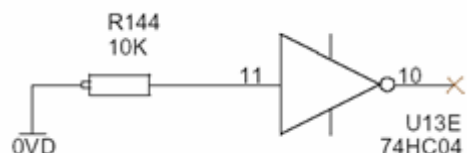
In order to avoid situations like the previously described ones, follow the criteria listed below during the board design:

- Use pull down resistors, instead of connecting the pin directly to the ground.
- Use pull up resistors instead of connecting the pin directly to the power supplies.
- Use resistances in series for the signals that are connected in the output to many digital components. In this way, the fan out of the single components will not be damaged.
- Use components whose outputs can be set in “three-state”.
- Connect the control pins (“Enable”, “Output enable”, ...) through a gate or pull/up or down resistors instead of connecting them directly to the power supplies or to the ground.
- The not used pins of one component must be tied to the power supplies or to the ground through one resistor.



All the pins of the components must be accessible; if not, it will not be possible to verify the proper soldering through the vectorless techniques (ElectroScan). This concerns also the pins of the component not used in the circuit.

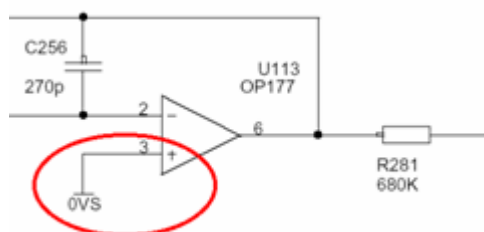
The input pins of the not used selections must be connected, through resistor, to the power supplies or to the ground.



## Analog integrated circuits

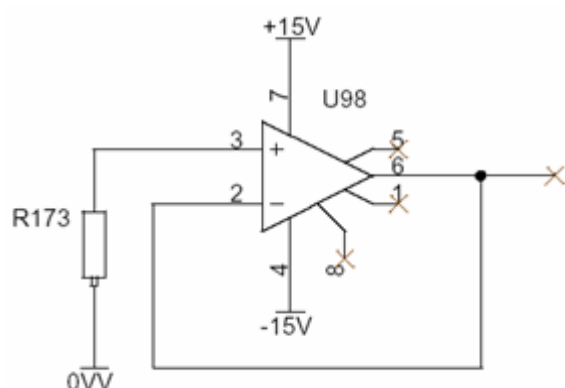
During In Circuit test, each component is tested individually, through special stimuli on its input and control pins.

This is the reason why it is not suggested to tie its pins directly to the power supplies or to the ground: in this case, the test system could not insulate them or control them.



The inputs of the sections not used should be connected, through resistor, to the ground or to the power supplies.

In case of operational amplifiers, it is suggested to connect the inverting input to the output too, in order to check the functioning of the section with "voltage follower" configuration.



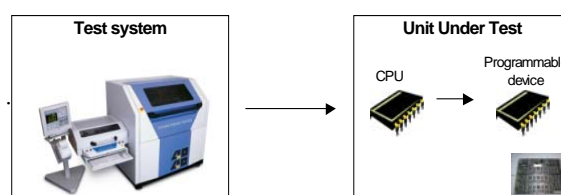
## On Board Programming

There are two ways to have access to the components to be programmed, depending on the board project and on the type of product.

### In System Write

In this case the programmable component is connected only to the board CPU.

The test system cannot have direct access to all the signals needed for the programming.



In this case, the component is programmed through the board CPU.

The test system talks with the CPU which provides the programming of the component.

### Direct programming

In this case, the programmable component can be accessed directly by the test system.

The CPU on board can be disabled or set in a known condition before starting the programming sequence.



The test system generates the commands, the voltages, the control signals and all what is needed by the component programming.

### Disabling the microprocessor

If one microprocessor is on the board to be programmed, before starting programming the component, it is necessary to set it in a defined and known state.



## Rules for the electric design

### Signals accessibility

Aside from the employed OBP programming type ("In system write" or "Direct programming") the nets where it is necessary to force or measure the signals must be accessible.



If the number of available signals is higher than the number of available probes (4), during the phase of design, it is possible to provide for a connector devoted to the programming; on this connector also the power supplies should be lead.

In this way, the OBP unit will be directly connected to the connector to enable the programming.



For what concerns the arrangement of the connector, it is important to pay attention to the directions defined in the chapter concerning the contact points arrangement.

If there is the intention to arrange some test pads in order to develop a bed of nails adapter devoted to the programming, it is necessary to follow the directions of the "Directions for the mechanical design" chapter.

## ECO

ECO is the acronym of "Engineering Change Order", or of all the modifications performed after the product issue in production.



Usually, it concerns needed simple modifications (tracks shearing, wirings or value change) not requiring a total project review.

During this phase, the designer can consider some aspects that can reduce to the minimum their impact on systems already existing (machines, programs, ...).

It is important to follow the rules listed below (the designer can easily manage them):

- Avoid moving the test pads
- If it is not strictly necessary, avoid moving the components
- Provide for the added components total accessibility





## Boundary Scan

### Boundary Scan Infrastructure

It is very important to observe some simple rules when constructing the boundary scans chains on design:

### Boundary-scan chain

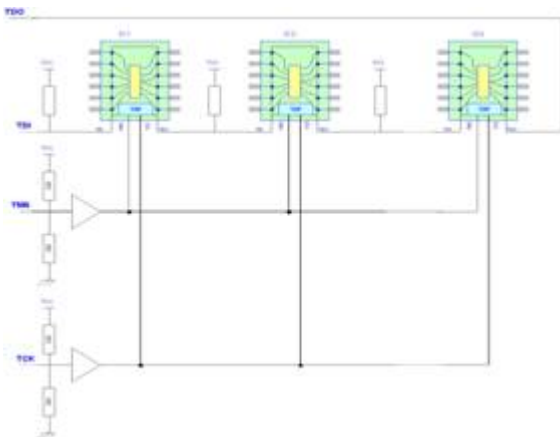
Place all devices in a single chain, simplifies connection to the board and simplifies the components test.

### Fully IEEE-1149.1 compliant devices

Before placing a component in a boundary-scan chain together to the devices on board, verify that the component fully complies with the IEEE-1149.1 standard.

### TAP signal noise

Provisions should be made to ensure that the signal quality of Test Access Port (TAP) signals on board, such as TCK, is maintained. Are recommended the following signal terminations on the board TAP signals:



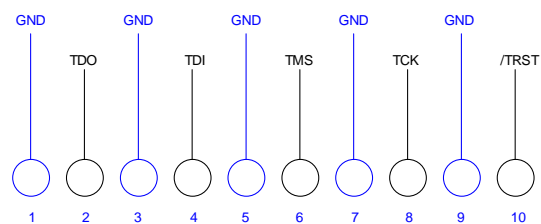
Signal	Direction	Termination
TRSTn	Input to the UUT	1K pull-up
TDI	Input to the UUT	1K pull-up
TDO	Output of the UUT	33 ohm series
TMS	Input to the UUT	1K pull-up
TCK	Input to the UUT	1K pull-up

Using these values of signal terminations has been shown to be very effective in reducing noise and signal integrity problems on the many designs tested with boundary-scan method.

When there are a large number of boundary-scan devices on board, it may be necessary to buffer the common TAP signals. Provide separate buffered signals to boundary-scan group of components on board, to reduce the loading on these signals.

### Boundary-scan chain connection

For connection to the boundary-scan chain on board, is recommended a 10-pin connector that contains the 5 TAP signals and 5 grounds alternate between them.



### Let Boundary-scan chain breakable

Can be helpful to keep boundary-scan components isolated in a chain by themselves. This can be done using jumpers or through the addition of electronic components, such as gates or multiplexers, to the board design.

The solution using logic (multiplexers) instead of jumpers, allows you to control the JTAG chain configuration based on the cable that is plugged into the JTAG connector.

## Board level design

In order to ensure maximum testability through boundary-scan, it is important to follow some rules when designing your board for boundary-scan test. General rules to follow to ensure that your design is testable through boundary-scan:

### TCK clock quality

The entire operations of the boundary scan circuits depend on the quality of the TCK signal. Distributing the TCK clock signal to all the boundary scan devices on the board requires special attention. Basically, in general the TCK signal needs to be treated like any other high-speed clock signal on the board. Use the same high-speed signal distribution guidelines that you apply to any other clock signal on your target board. Pay attention to: loading, termination, distribution, layout-routing, matching trace impedance to termination resistor, keeping the clock trace as short as possible, etc. The following are some of the issues that should be considered by the circuit designer when designing for testability:

1. When buffering the TCK signal do NOT use PLL based clock buffer chips. Zero delay clock distribution devices (for distributing the TCK signal to multiple devices on the board) always incorporate internal PLL and cannot be used. Unlike CPU clocks and system clocks, the TCK clock is not free running.
2. Add series resistors on clock driver's outputs.
3. The size of the board and the number of boundary-scan compatible components may require separate TCK signal buffers for each group of physically adjacently boundary-scan devices.
4. Adding buffers on the TCK (and the other TAP signals) will decrease the maximum TCK clock rate that can be used for scanning.
5. The other TAP signal is less sensitive and the 1K pull-up generally suffice and typically no other special considerations are required.

### Power Supply filtering

Boundary-scan test sometimes places additional constraints on board design. When all components enter in a specific test state, a large number of outputs on-board may change state simultaneously (more than during normal operation). This can induce ground bounce or other circuit problems when the devices on-board are not properly bypassed.

Take in special care this condition in your design to avoid its harmful event so ensure proper components filtering.

### BSDL file availability

Use components that have a BSDL file available. So during the component selection phase, ensure that the manufacturer has created a BSDL file for any JTAG components that intend to use in the design. BSDL is the standard language for describing boundary-scan devices and device manufacturers usually provides a BSDL for the component as soon as engineering samples are available.

Typically, you can get BSDL files from the component manufacturer's web site.

### Met compliance enable conditions

The compliance enable description in the BSDL file, indicates the component pin states that must be maintained in order for the TAP and test logic in the component to be operational. For example, in the BSDL file for the Motorola MCF5272 device, the following Compliance Enable description is provided:

```
Attribute COMPLIANCE_PATTERNS of
MCF5272_1K75N: entity is      "(HIZ) (1)";
```

This indicates that the pin "HIZ" on the MCF5272 component must be held in a high state in order for the TAP and test logic in the component to operate in a consistent way with that described in the IEEE-1149.1 standard. In BSDL files generated under earlier versions of BSDL, this may have been described through a COMPLIANCE\_ENABLE statement.

For testability of the boundary-scan chain on board, must be met the compliance enable conditions listed in the BSDL file. Is mandatory connects the listed pins to a connector or any accessible Test Point.

### Pin numbering in board netlist

In order to have Automatic Test Pattern Generation of boundary-scan test vectors, correct pin numbers in the board netlist must be used. For all the boundary-scan components used on board, their component pin numbers in the board netlist must exactly match the pin numbers in the BSDL files. Manufacturer standard pin numbering should be used for the component in the netlist.

## Rules for the electric design

### CAD files

The words “CAD file” refer to the information used by the CAD/CAE systems for the design of the electric diagrams and of the PCB.

Atos2, the 4040 operating system, uses the CAD files for the test program automatic generation. Their format is stored in one or many ASCII text files.

The CAD files formats that can be accepted and used depend on the CAD/CAE system used; the formats supported by SPEA are listed in the technical note entitled “ATOS2 – Board CAD data” (code: 81280001.056).

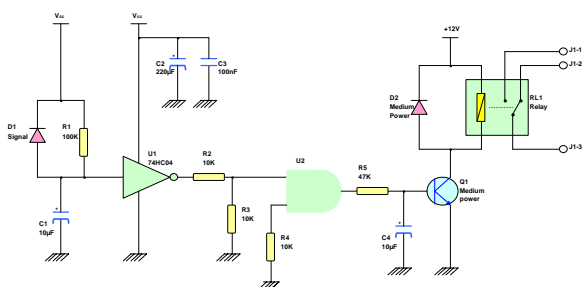
The information needed for the automatic test program generation are available in the:

- Part list
- Net list
- Coordinate list
- Access list
- Track list

The part list, which is defined sometimes as “Bill of Materials” is a text file in ASCII format: it contains the list of all the parts used for the board assembly. It must contain: drawing reference, part number, value, tolerance, ...

The net list, which is also defined “wirelist” is an ASCII file generated by the CAD/CAE system, containing the information about the interconnection of the components.

In substance, it represents the electrical diagrams.



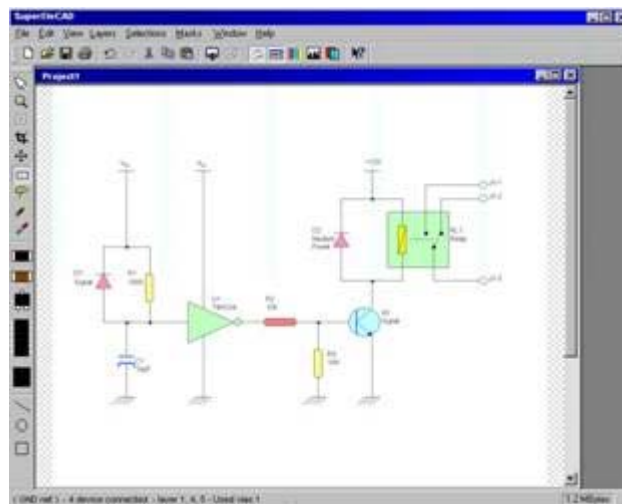
The coordinate list contains, for each pin of the components, the information concerning their physical position (X and Y coordinates).

The information concerning the access of the contact points of the board are available in the access list.

The track list contains the information concerning the layout and the characteristics of the tracks of the PCB.

### Supported CAD formats

Every CAD/CAE system has its own output format; for this reason SPEA developed a specific import for the formats that are market-standard as, for example, Cadence, Mentor, Verybest, Pads, Zuken, ...



Some of the CAD formats supported by SPEA are:

- CadStar
- Zuken
- Visual
- DDE
- S E-CAD
- GenCad
- Mentor
- Pads
- Protel
- Cadence Allegro
- Integra
- TXF-Out
- Verybest

The update list of the supported CAD formats is available in the document “ATOS2 – Board CAD data” cod. 81280001.056



# OVERVIEW

## **Design for Testability milestones**

It is important to pay attention to the fact that the minimum dimensions defined in this document are referred to the 4040 model "Top-of-class", the state-of-art flying probe.

For the other flying probe models ("High Precision" and "Very High Precision") the minimum dimensions change with the system characteristics.



	Suggested dimensions	Minimum dimensions
Square test pad dimensions	1x1 mm	80x80 $\mu$ m
Round test pad diameter	1 mm	80 $\mu$ m
Test pad outline	Square	
Via external diameter	1 mm	
Via metallization thickness		100 $\mu$ m
Pitch among test points	1 mm	250 $\mu$ m
Length of the soldering pads for IC SMT	400 $\mu$ m	100 $\mu$ m
Width of the soldering pads for IC SMT	400 $\mu$ m	100 $\mu$ m
Fiducial outline	Square, rounded or cross-shaped	
Dimensions of the free space around the fiducial	11x9 mm	
Dimensions of the area devoted to the fiducial (free from other parts)	1 mm <sup>2</sup>	
Dimensions of the area, fiducial included	3x3 mm	1.5x1.5 mm
Maximum dimensions of the area, fiducial included	4.5x4.5 mm	
Area free from contact points around components 5mm high	2x2 mm	1.4x1.4 mm
Area free from contact points around components 10mm high	3x3 mm	2.8x2.8 mm
Area free from contact points around components 15mm high	4.5x4.5 mm	4.2x4.2 mm
Area free from contact points around components 20mm high	6x6 mm	5.6x5.6 mm
Area free from contact points around components 25mm high	7.5x7.5 mm	7.0x7.0 mm
Area free from contact points around components 30mm high	9x9 mm	8.4x8.4 mm
Area free from contact points around components 35mm high	10x10 mm	9.8x9.8 mm
Height of the components of the tested side (maximum)	55 mm	
Height of the components of the side opposite to the tested one (maximum)	110 mm	
Weight of the board for the conveyance on standard automatic line	$\leq 1500$ g	
Dimensions of the space free from components on the board edge for the conveyance <sup>1</sup>		3 mm for the length of the board
Dimensions of the area free from components as to the board edge for the locking <sup>2</sup>		7x15 mm
Number of boards in a panel (maximum)	128	

<sup>1</sup>= For systems equipped with IBL

<sup>2</sup>= For systems equipped with SBL, for every locking point **29**

Arrange at least 2 contact points for each net connected to:

- Capacity ( $\geq 10\mu\text{F}$ )
- Resistances ( $\leq 100\Omega$ )
- Diodes low-medium power
- Leds
- Zeners
- Bipolar transistors
- Mos-Fet transistor
- Relays
- Transformers
- Inductances
- Power supplies



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